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ADP013351

TITLE: The Effects of Plasma Induced Damage on the Channel Layers of Ion Implanted GaAs MESFETs during Reactive Ion Etching [RIE] and Plasma Ashing Processes

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TITLE: Materials Research Society Symposium Proceedings; Volume 720. Materials Issues for Tunable RF and Microwave Devices III Held in San Francisco, California on April 2-3, 2002

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The Effects of Plasma Induced Damage on The Channel Layers of Ion Implanted GaAs MESFETs during Reactive Ion Etching(RIE) and Plasma Ashing Processes

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ABSTRACT

The gate length of GaAs MESFETs is required to be shorter for higher microwave frequency applications. The side-wall process using silicon nitride is one of the effective processes to fabricate short gate length GaAs MESFETs. The side-wall process consists of deposition and anisotropic etching of silicon nitride and delivers plasma induced damages on the channel layers of the devices. In this study, the effects of plasma induced damage on the channel layers of ion implanted GaAs MESFETs during reactive ion etching and plasma ashing processes have been investigated. The plasma induced damage was characterized by sheet resistance measurement, X-ray photoelectron spectroscopy(XPS) and auger electron spectroscopy(AES) of different etched surfaces, compared with a chemically wet-etched reference surface. Also the effect of the plasma induced damage on the device performance was investigated. As a result, plasma ashing can deteriorate the plasma-induced damage by RIE.

INTRODUCTION

GaAs MESFETs have been widely used in the microwave frequency application. Recently, as a higher frequency application is demanded, shorter gate length GaAs MESFETs should be fabricated through appropriate processes such as the side wall process using silicon nitride. The side wall process includes plasma-related processes such as reactive ion etching (RIE) and plasma ashing which are generally used due to the advantages of anisotropic etching profile and clean surface. However, these processes are usually accompanied with the plasma induced damage and contamination on the channel layers, which cause the degradation of the device performance. In this paper, the damaged layer has been characterized by X-ray photoelectron spectroscopy (XPS) and auger electron spectroscopy (AES). The effects of the plasma induced damage on the performance of GaAs based devices were also discussed.

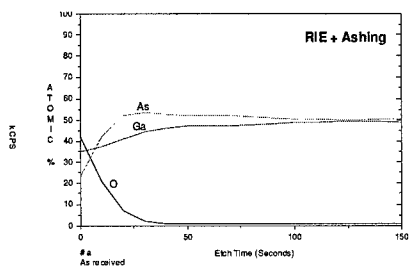
EXPERIMENTAL DETAILS

For the experiment, liquid-encapsulated-czochralski (LEC) grown semi-insulating GaAs (100) wafers were used. To get the abrupt and shallow channel layers, Be implantation was performed at 40KeV and $2 \times 10^{-2} \text{cm}^{-2}$ before Si implantation at 60KeV and $7 \times 10^{-2} \text{cm}^{-2}$. Doped Si and Be were electrically activated by rapid thermal annealing at 900°C with the wafer capped by silicon nitride. All samples were dipped in HF solution to remove the silicon nitride after the activation and a new silicon nitride was deposited on the front side of the samples. AuGe/Ni/Au source/drain ohmic contacts were formed by thermal evaporation and rapid thermal annealing at 380°C for only GaAs MESFET samples. In this study, two kinds of gate region processes were performed. Generally, after the 0.35µm gate length was defined by using I-line optical stepper, the silicon nitride capping layer was etched by reactive ion etching (CF_4/O_2 plasma) at 30mTorr until it was completely removed. Photo resist was removed by plasma ashing (N_2/O_2 plasma) for 10 minutes at 500mTorr. The gate recess etching was performed in $\text{H}_3\text{PO}_4 + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ (4:1:180) solution and a first-level metal (Ti/Pt/Au) on the recessed region was patterned by lift-off. However, we modified the gate region process because the microwave ashing may cause the plasma induced damage on the channel layers. When the silicon nitride was etched by RIE, the capping layer was remained as much as 250Å in the thickness so that microwave ashing should be performed with the channel layer capped. After the remained silicon nitride was removed by RIE, the same recess etching and metalization processes were followed. Three kinds of analysis samples were prepared without patterning. One sample was treated by RIE and microwave ashing, another by RIE and the other by wet etching(BOE 6:1). Surfaces of the analysis samples were analyzed by X-ray photoelectron spectroscopy (XPS), auger electron spectroscopy (AES) and contactless sheet resistance measurement. XPS and AES analysis were performed by using each the VG scientific ESCALAB 200R and the VG scientific MICROLAB 310D(X-ray source : Al-K α). XPS data were calibrated to 284.8eV carbon 1s peak.

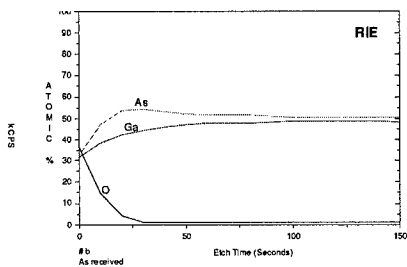
RESULT AND DISCUSSION

Surface analysis

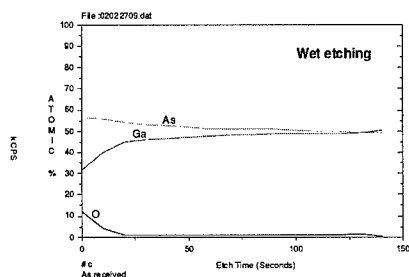
GaAs surfaces were analyzed by auger electron spectroscopy (AES) and X-ray photoelectron spectroscopy (XPS) to characterize the surface contamination, the stoichiometry and the chemical bonding. Surface of a chemically wet etched sample (HF solution) was used as a reference. Fig 1 shows AES depth profile of the channel layers for different etching conditions of silicon nitride on



(a)



(b)



(c)

Fig. 1 AES depth profile of GaAs samples for (a) RIE + ashing, (b) RIE and (c) wet etching of silicon nitride on GaAs substrate.

GaAs substrate. Oxygen content of the surface in the RIE treated sample was larger than that in the wet etched sample and oxygen existed more deeply in the RIE-treated sample than that in the wet-etched sample. Arsine content of the surface in the RIE treated sample was smaller than that in the wet etched sample. (Fig. 1 (b), (c)) Microwave ashing increased these effects. (Fig.1(a)) Fig. 2 shows Ga-3d and As-3d XPS signal of GaAs surface. After RIE, the Ga 3d peak broadened on the high binding energy of Ga-oxide (Ga_2O_3) and the maximum peak position of the Ga 3d peak also shifted to the high binding energy. (Fig 2. (c), (e)) The As 3d peak of low binding energy of GaAs also broadened and the peak intensity of high binding energy (As_2O_3 , As_2O_5) relative to the intensity of low binding energy (GaAs) increased. (Fig 2. (d), (f)) [1]. This difference in the degree of oxidation between the RIE treated sample and the wet etched sample may be attributed to the formation of highly reactive porous surface by RIE.[2] This means that GaAs was oxidized in the upper side of the channel and some portion of the channel layer was changed to the GaAs-oxide. Fig 2(a), (b) shows that the damage layer induced by RIE is more

reactive in the microwave ashing plasma than in the air. The degradations of the RIE treated samples led to the increase of the sheet resistance in GaAs MESFET channel layer from 930ohm/sq to 1070 ohm/sq. Microwave ashing of the RIE treated sample delivered an additional increase as much as about 260ohm/sq.

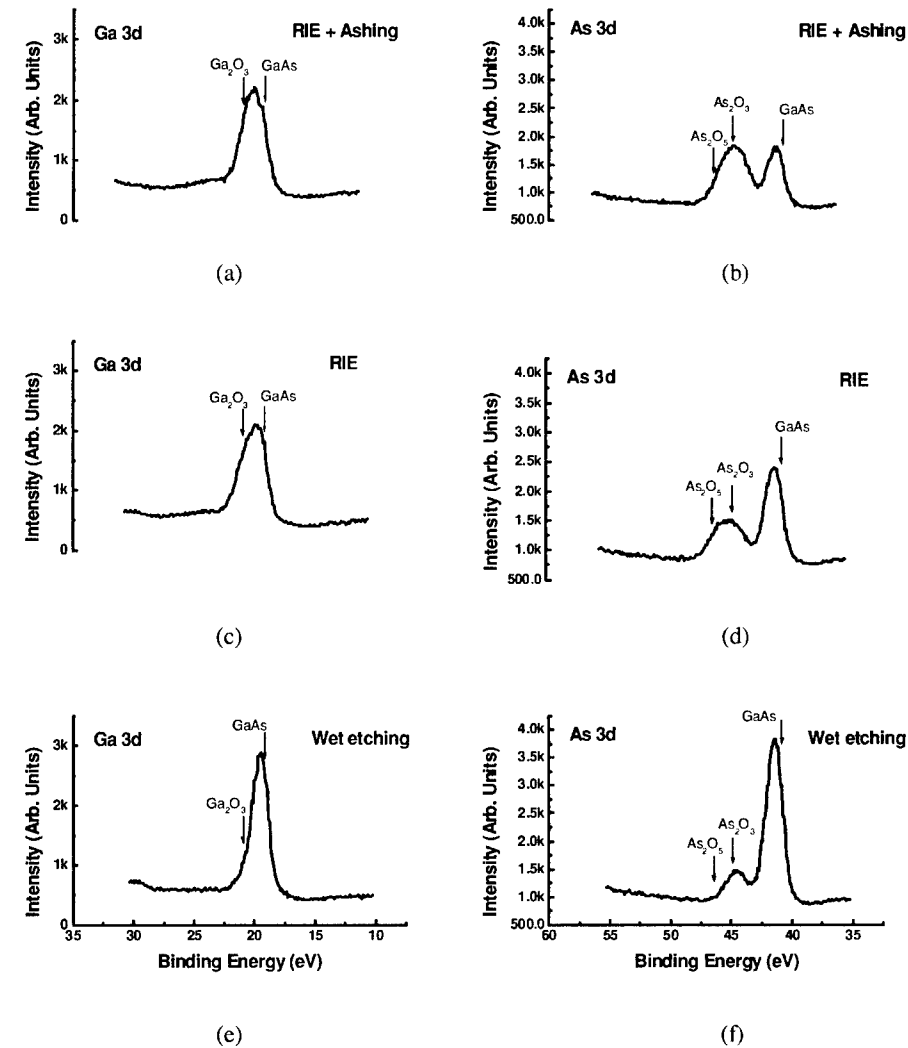


Fig 2. Ga 3d and As 3d XPS signal of GaAs samples for RIE + ashing, RIE and wet etching of silicon nitride on GaAs substrate.

MESFET performance

RIE process was performed to open the gate region, followed by microwave ashing in order to remove photo resist. RIE process decreased the slope of I-V and the saturated channel current from 90mA to 80.6mA, corresponding to the increase of the sheet resistance in the channel layer after RIE. These damages are attributed to the formation of the oxide layer in the upper side of the channel layer during RIE . Microwave ashing caused the additional decrease as much as 20.2mA in the saturated current. Fig 3 shows I-V characteristics after the gate metalization without recess etching. After microwave ashing, the slope of I-V curve and the saturated current level decreased, corresponding to the additional increase of sheet resistance in the channel layer due to the increased degradation, such as the GaAs oxidation, induced by microwave ashing. [3]

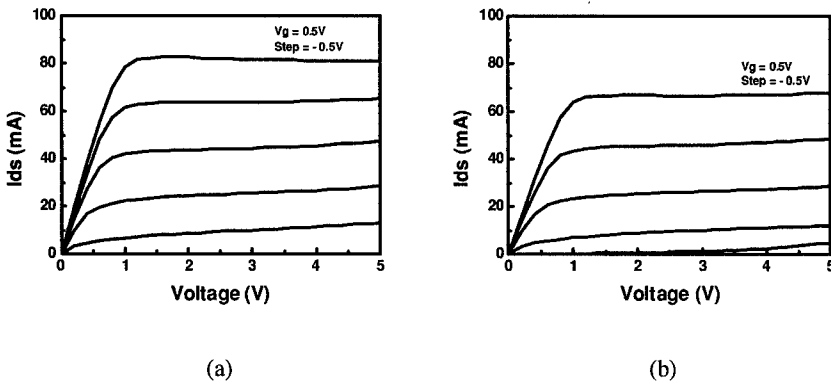


Fig 3. I-V characteristics for different etching conditions of silicon nitride, (a) RIE and (b) RIE + Ashing.

Depletion-mode MESFETs were fabricated in order to show the effect of microwave ashing on the performance of GaAs MESFETs. The ashing-exposed channel layer was recessed for 40sec and the capped channel layer was recessed for 70sec. After the gate recess etching, two channels had the same current level. The ashing-exposed MESFET showed the shift of threshold voltage from $-0.66V$ to $-0.59V$ and the longer tail of transconductance line in Fig 4. The reverse saturation current of the gate/n-GaAs schottky contact in the capped MESFET ($J_0 = 0.702pA$) was smaller than that in the ashing-exposed MESFET ($J_0 = 4.53pA$), indicating that the barrier height of the gate/n-GaAs schottky contact in the capped MESFET was higher than that in the ashing-exposed MESFET. The increased oxidation of GaAs in some portion of the channel layer by microwave ashing led to the reduction of the barrier height, evident from the reduction of the drain source current at V_{gs} (gate-source voltage) = $0V$. When the capped channel layer was

recessed for 60sec, the MESFET with 60sec channel recess etching had the same threshold voltage ($V_{th} = -0.66V$) as the ashing-exposed MESFET. However, the drain-source current in the former MESFET was larger than that in the latter MESFET. Therefore, Fig 4 shows that the channel of the capped MESFET pinches off more easily if both the ashing-exposed MESFET and the capped MESFET have the same drain-source current at V_{gs} (gate-source voltage) = 0V.

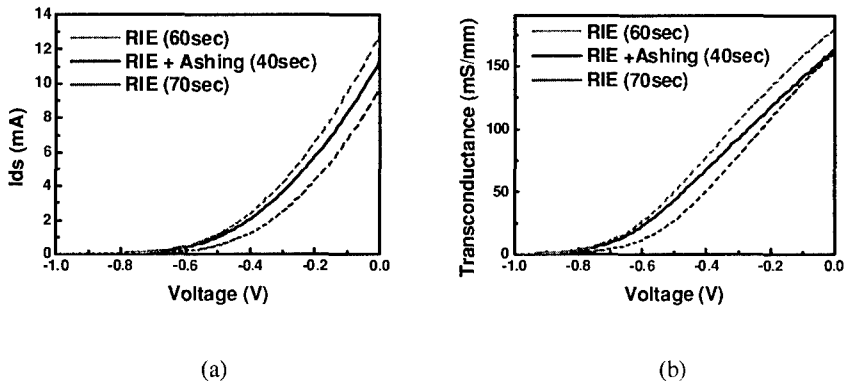


Fig 4. Transconductance and the drain-source current as a function of the gate-source voltage for different process conditions.

CONCLUSION

After the RIE treatment, the oxidation of GaAs surface increased and some portion of the channel layer was changed into GaAs-oxide such as Ga_2O_3 , As_2O_3 and As_2O_5 . The Arsine was depleted in GaAs surface during RIE process. These effects increased by the additional microwave ashing of the RIE treated GaAs surface. The RIE damage led to the reduction of the channel current. The additional microwave ashing delivered the reduction of the barrier height in the gate / n-GaAs schottky contact and deteriorated the pinch-off characteristics of GaAs MESFET.

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